FP6601Q

USB Dedicated Charging Port Controller for Fast Charging Protocol and QC 2.0/3.0

Description

The FP6601Q is a fast charge protocol controller for HiSilicon Fast Charging Protocol (FCP) and Qualcomm® Quick Charge™ 2.0/3.0 (QC 2.0/3.0) USB interface. The device can fast charging FCP or QC 2.0/3.0 powered device (PD). The protocol feature monitors USB D+/D- data line voltage or D- data line transmission and automatically adjusts output voltage of power bank and wall adaptor to optimize charge time.

FP6601Q can support not only USB BC compliant devices, but also Apple / Samsung / HUAWEI devices and automatically detects whether a connected powered device is QC 2.0/3.0 or FCP capable before enabling output voltage adjustment. If a PD not compliant to QC 2.0/3.0 or FCP is detected the FP6601Q disables output voltage adjustment to ensure safe operation with legacy 5 V only USB PDs.

The FP6601Q is available in a space-saving SOT-23-6 package.

Features

- Support HiSilicon Fast Charging Protocol (FCP) for Output Voltage and Current Communication
- Support Qualcomm® Quick Charge™ 2.0/3.0
  - Class A : 3.6V up to 12V Output Voltage
- Automatic Selection FCP and QC2.0/3.0 Protocols
- Supports USB DCP Shorting D+ Line to D- Line per USB Battery Charging Specification, Revision 1.2
- Meets Chinese Telecommunication Industrial Standard YD/T 1591-2009
- Supports USB DCP Applying 2.7V on D+ Line and 2.7V on D- Line
- Supports USB DCP Applying 1.2V on D+ and D- Lines
- SOT-23-6 Package
- UL Certification No. 4787452994-2

Applications

- Wall-Adapter, Smart Phones, Tablets, Notebooks
- Mobile / Tablet Power Bank
- Car Charger
- USB Power Output Ports

Pin Assignments

S6 Package(SOT-23-6)

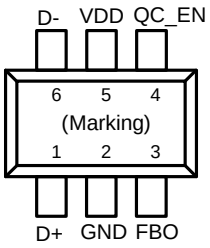


Figure 1. Pin Assignment of FP6601Q

Ordering Information

FP6601Q□

Package Type
S6: SOT-23-6

SOT-23-6 Marking

Part Number	Product Code
FP6601QS6	**FT4**

Typical Application Circuit

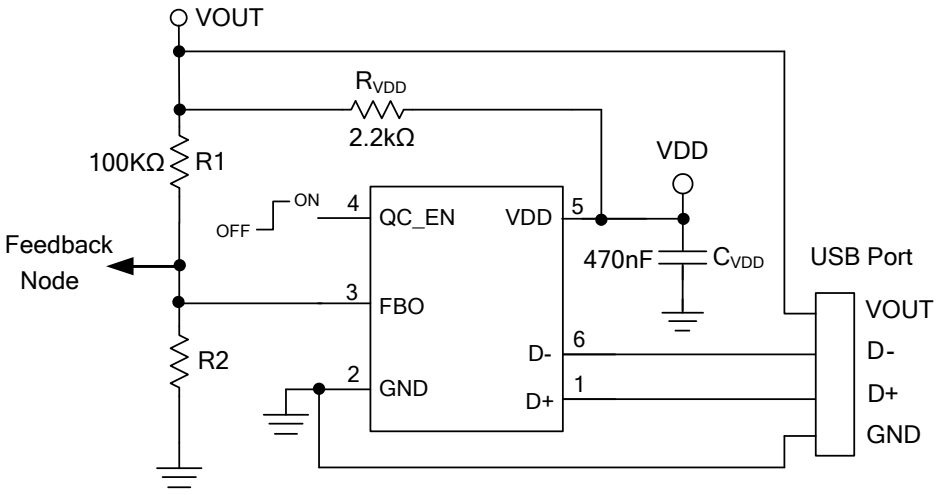


Figure 2. Typical Application Schematic

Output Voltage Lookup Table(QC 2.0/3.0)

D+	D-	Output Voltage
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	Continuous mode
0.6V	High-Z	5V (Default)

Functional Pin Description

Pin Name	Pin No. (SOT-23-6)	Pin Function
D+	1	USB D+ data line input pin. Recommended this pin connect without resistors(open) or with a resistor higher than 1MΩ connect to GND.
GND	2	Ground pin.
FBO	3	Feedback output pin. Current Sink/Source FB Node.
QC_EN	4	QC_Enable: High-Z with QC2.0/3.0 and FCP function; logic low disable QC2.0/3.0 and FCP function.
VDD	5	Power supply input pin.
D-	6	USB D- data line input pin.

Block Diagram

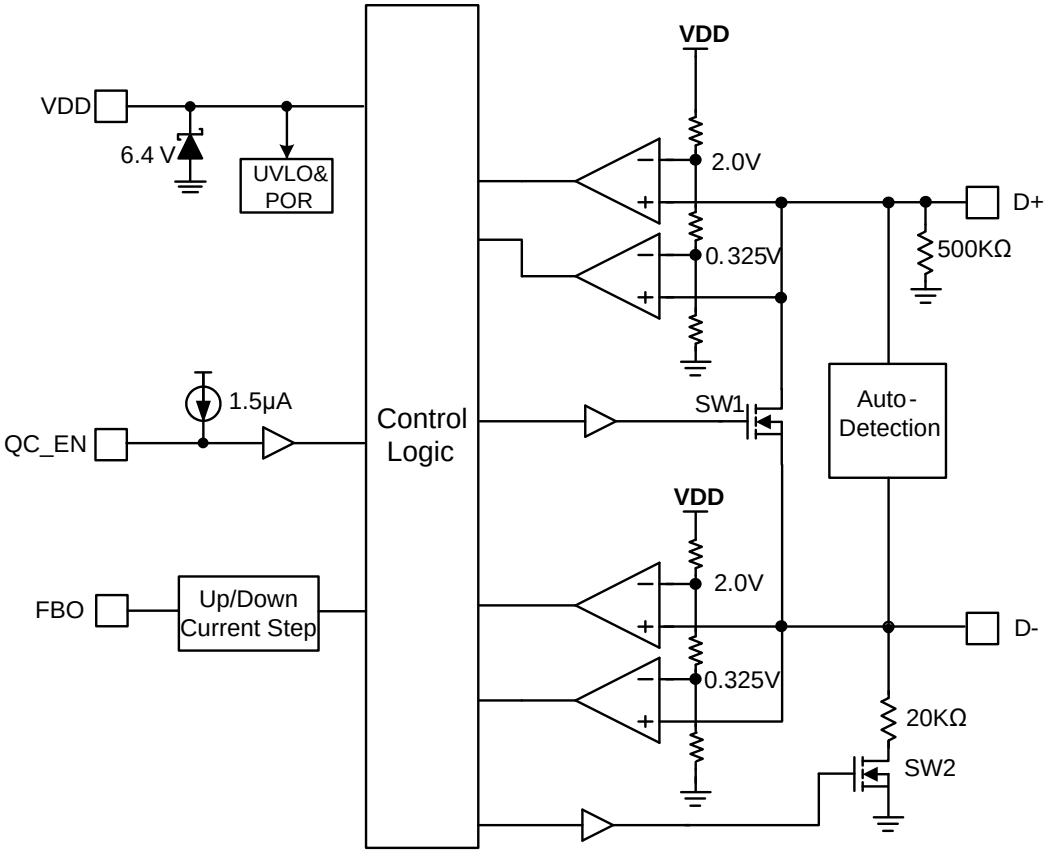


Figure 3. Block Diagram of FP6601Q

Absolute Maximum Ratings (Note 1)

- Input Supply Voltage VDD ---------- - 0.3V to + 6.5V
- All Other Pins Voltage ---------- - 0.3V to + 6.5V
- Maximum Junction Temperature (T_J)---------- + 150℃
- Storage Temperature (T_S)---------- - 65℃ to + 150℃
- Lead Temperature (Soldering, 10sec.) ---------- +260°C
- Power Dissipation @T_A=25℃, (P_D)

  SOT-23-6---------- 0.5W
- Package Thermal Resistance, (θ_{JA}) (Note 2)

  SOT-23-6---------- 250°C/W
- Package Thermal Resistance, (θ_{JC})

  SOT-23-6---------- 110°C/W

Note 1：Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.
Note 2：θ_{JA} is measured at 25°C ambient with the component mounted on a high effective thermal conductivity test board of JEDEC-51-7.

Recommended Operating Conditions

- Input Supply Voltage (VDD)---------- 3.2V to 6.4V
- Operation Temperature Range (T_{OPR}) ---------- -40°C to +85°C

Note 3：Over operating free-air temperature range (unless otherwise noted)

Electrical Characteristics

(VDD=5V, T_A=25℃ and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Power						
VDD Input Voltage Range	V_{DD}		3.2		6.4	V
Input UVLO Threshold	$V_{UVLO(VTH)}$	V_{DD} Falling	2.5		2.9	V
VDD Supply Current		V_{DD} =5V, Measure V_{DD}		200		μA
VDD Shunt Voltage	$V_{DD(SHUNT)}$	IV_{DD} = 3mA	5.9	6.4	6.8	V
High Voltage Dedicated Charging Port (HVDCP)						
Data Detect Voltage	$V_{DAT(REF)}$		0.25	0.325	0.4	V
Output Voltage Selection Reference	V_{SEL_REF}		1.8	2.0	2.2	V
D+ High Glitch Filter Time	$T_{GLITCH(BC)-D+\_H}$		1000	1250	1500	ms
D- Low Glitch Filter Time	$T_{GLITCH(BC)-D-\_L}$			1		ms
Output Voltage Glitch Filter Time	$T_{GLITCH(V)CHANGE}$		20	40	60	ms
D- Pull-Down Resistance	$R_{D-(DWN)}$			20		kΩ
Continuous Mode Glitch Filter Time (Note 4)	$T_{GLITCH-CONT-CHANGE}$		100		200	μs
D+ Leakage Resistance	$R_{DAT-LKG}$	V_{DD} =3.2-6.4V,VD+=0.6-3.6V Switch SW1=Off	300	500	800	kΩ
Switch SW1 On-Resistance	$R_{DS\_ON\_N1}$	V_{DD} =5V,SW1= 200μA			40	Ω
Up/Down Current Step	I_{UP}, I_{DOWN}	I_{UP} = 40μA (9V), 70μA (12V), I_{DOWN} = 14μA (3.6V)		2		μA
DCP 1.2V Charging Mode						
$D+_{\_1.2V}$/$D-_{\_1.2V}$ Line Output Voltage			1.08	1.2	1.32	V
$D+_{\_1.2V}$/$D-_{\_1.2V}$ Line Output Impedance				100		kΩ
Apple 2.4A Mode						
$D+_{\_2.7V}$/$D-_{\_2.7V}$ Line Output Voltage			2.57	2.7	2.84	V
$D+_{\_2.7V}$/$D-_{\_2.7V}$ Line Output Impedance				33.6		kΩ
D- SECTION (FCP)						
D- FCP Tx Valid Output High	V_{TX-VOH}		2.55		3.6	V
D- FCP Tx Valid Output Low	V_{TX-VOL}				0.3	V
D- FCP Rx Valid Output High	V_{RX-VIH}		1.4		3.6	V
D- FCP Rx Valid Output Low	V_{RX-VIL}				1.0	V

Electrical Characteristics (Continued)

(VDD=5V, T_A=25℃ and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
D- Output Pull-Low Resistance (FCP) (Note 4)	R_{PD}		400	500	600	Ω
Unit Interval For FCP PHY Communication	UI	f_{CLK} = 125kHz	144	160	180	μs

Note 4：Not production tested.

Application Information

Function Description

The FP6601Q is a USB high voltage dedicated charging port interface IC for Qualcomm® Quick Charge™ 2.0/3.0 class A, HiSilicon FCP specification.

The FP6601Q is a USB Dedicated Charging Port Controller can fast charge most of the handheld devices. It can be like the original charging adapter. The FP6601Q can support BC1.2, Apple, Samsung and HUAWEI.

It also supports full output voltage range of QC 3.0 Class A(3.6V to 12V) or QC 2.0 Class A(5V,9V,12V)

Quick Charge 2.0/3.0 Interface

Power up D+/D- is supply 2.7V to Apple Device and then supply D+ short to D- into BC1.2. Set the output voltage level 5V. If D+ continuous above 0.325V and keep 1.25 seconds FP6601Q can automatic choose into Quick Charge 2.0/3.0, FCP operation mode.

When $V_{DAT(REF)}$< D+ <V_{SEL_REF} and D- > V_{SEL_REF} , the FP6601Q enter continuous mode. Each step D+ from 1V to 3V Pulse-width during 200us cause current sink 2uA by FBO. The maximum output sink current is 70uA for output voltage reach to 12V.

Each step D- from 3V to 1V Pulse-width during 200us cause current source 2uA by FBO. The minimum output source current is 14uA for output voltage reach to 3.6V.

If PD without QC 2.0 the device will keep output voltage level 5V guarantee safe operation for only 5V USB PD. When USB cable unplug the D+ voltage < $V_{DAT(REF)}$ and output voltage recovery default mode 5V.

Shunt Regulator

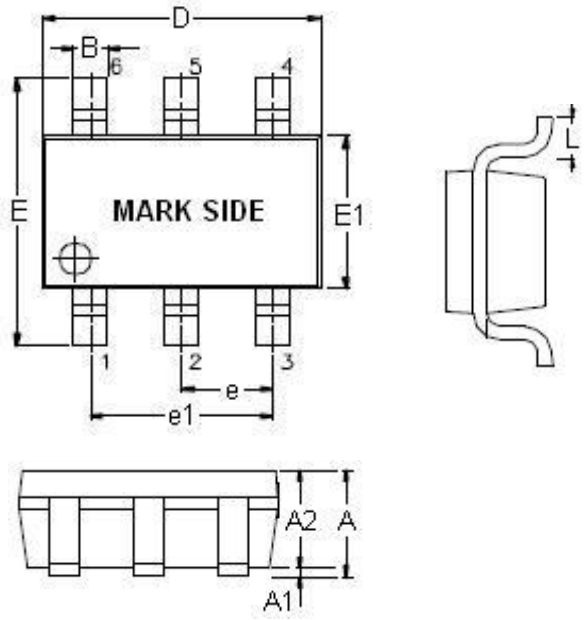
The wide power supply output voltage through external resistor from R_{VDD} to VDD. The internal with Zener-Diode clamp VDD pin at 6.4V. Recommend R_{VDD} =2.2kΩ and C_{VDD}=470nF.

QC_EN Function

When QC_EN pin disable QC 2.0/3.0,FCP function by connect to GND. Otherwise, enable function by connect to VDD or floating. QC_EN signal need to be ready before FP6601Q start detection. When FP6601Q already access QC2.0/3.0 or FCP mode, the mode won't be changed by setting QC_EN pin signal (High to Low).

Outline Information

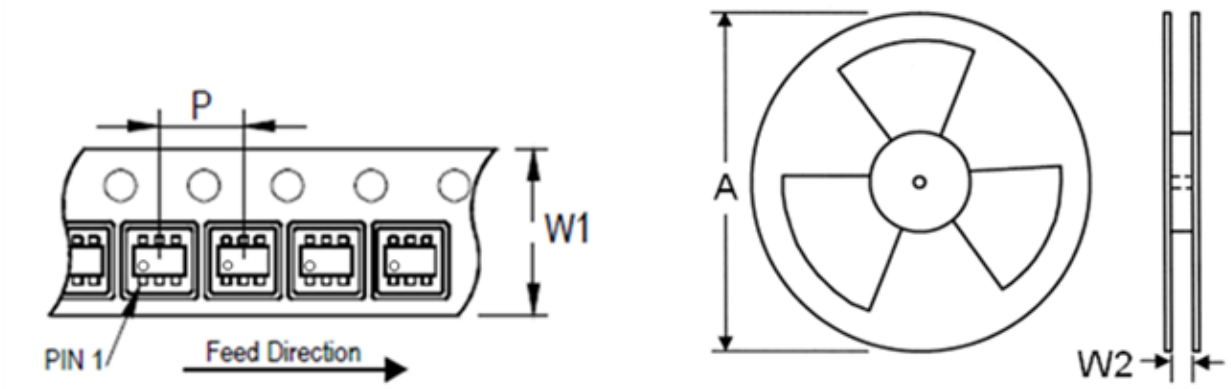
SOT-23-6 Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.30	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
L	0.30	0.60

Note：Followed From JEDEC MO-178-C.

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000