MT6328 PMIC Technical Brief

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Document Revision History

Revision	Date	Author	Description
1.0	2014-09-09	Luke Tsai	Initial draft

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1 Overview

1.1 Features

- Handles all 2G/3G/4G smart phone baseband power management
- Input range: 2.5 ~ 4.5V
- 5 buck converters and 28 LDOs optimized for specific 2G/3G/4G smart phone subsystems
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC.
- 32K RTC oscillator for system timing, 1.8 and 2.8V clock buffer output
- Flexibility for various configurations of indicator LED current source: 2 ISINK
- SPI interface
- Li-ion battery charging function
- USB Battery Charging Specification ver 1.1/1.2 (BC1.x) Compliance
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog reset
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- 206-pin VFBGA package

1.2 Applications

MT6328 is ideal for power management of 2G, 3G and 4G smart phones and other portable systems.

1.3 General Descriptions

MT6328 is a power management system chip optimized for 2G/3G/4G handsets and smart phones, containing 5 buck converters and 28 LDOs optimized for specific 2G/3G/4G smart phone subsystems.

LED drivers support up to 2 channels of LEDs with independent control. Flexible control includes register mode, PWM mode and breath mode.

Sophisticated controls are available for power-up, battery charging and the RTC alarm. MT6328 is optimized for maximum battery life, allowing the RTC circuit to stay alive without a battery for several hours.

MT6328 adopts SPI interface and 2 SRCLKEN control pins to control buck converters, LDOs, and various drivers; it provides enhanced safety control and protocol for handshaking with BB.

MT6328 is available in a 206-pin VFBGA package. The operating temperature ranges from -25 to +65°C.

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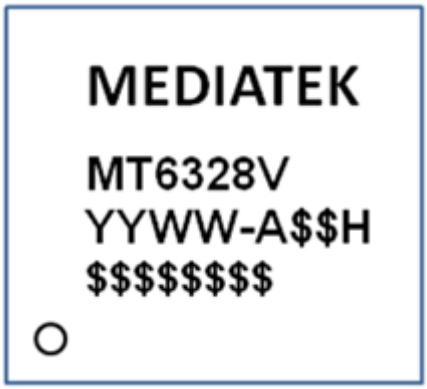
1.4 Ordering Information

Order #	Marking	Temp. range	Package
MT6328V/A		-25 ~ +65°C	VFBGA 206L

1.5 Top Marking Definition

MT6328V/A



YYWW: Date code
$: Random code

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1.6 Pin Assignments and Descriptions

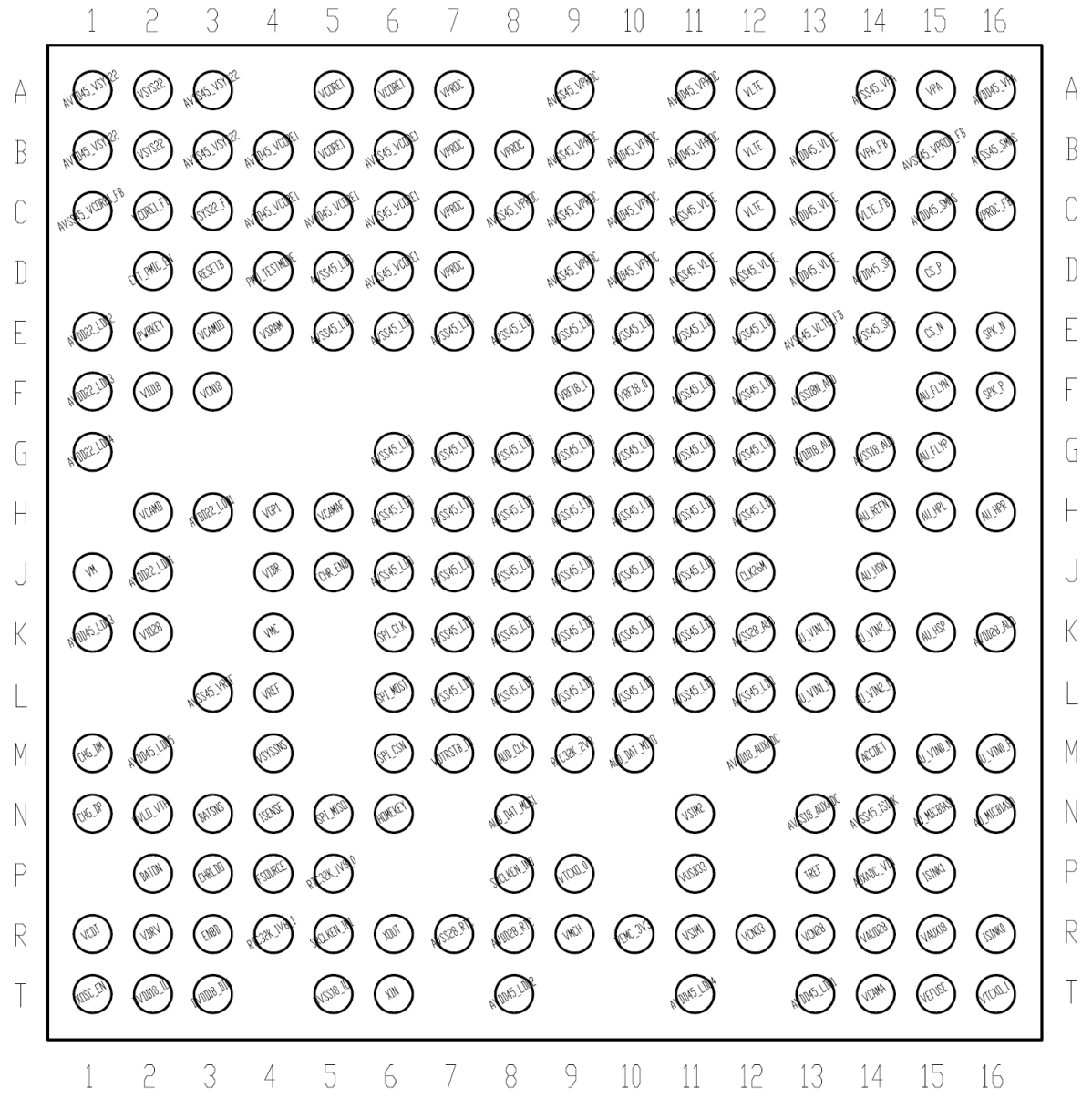

Figure 1-1. MT6328 VFBGA 206 (6.6x6.6mm) pin assignment

Table 1-1. MT6328 pin descriptions

Ball	Symbol	I/O	Description
A1,B1	AVDD45_VSYS22	PWR	Power supply of VSYS22
A2,B2	VSYS22	O	SW node of VSYS22
A3,B3	AVSS45_VSYS22	GND	VSYS22 ground
C3	VSYS22_FB	I	BUCK VSYS22 feedback pin
B4,C5,C4	AVDD45_VCORE1	PWR	Power supply of VCORE1

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Ball	Symbol	I/O	Description
A5,A6,B5	VCORE1	O	SW node of VCORE1
B6,C6,D6	AVSS45_VCORE1	GND	VCORE1 ground
C1	AVSS45_VCORE1_FB	I	Remote sense on ground of VCORE1
C2	VCORE1_FB	I	BUCK VCORE1 feedback pin
A11,B10,B11,C10,D10	AVDD45_VPROC	PWR	Power supply of VPROC
A7,B7,B8,C7,D7	VPROC	O	SW node of VPROC
A9,B9,C8,C9,D9	AVSS45_VPROC	GND	VPROC ground
B15	AVSS45_VPROC_FB	I	Remote sense on ground of VPROC
C16	VPROC_FB	I	BUCK VPROC feedback pin
B13,C13,D13	AVDD45_VLTE	PWR	Power supply of VLTE
A12,B12,C12	VLTE	O	SW node of VLTE
C11,D11,D12	AVSS45_VLTE	GND	VLTE ground
E13	AVSS45_VLTE_FB	I	Remote sense on ground of VLTE
C14	VLTE_FB	I	BUCK VLTE feedback pin
A16	AVDD45_VPA	PWR	Power supply of VPA
A15	VPA	O	SW node of VPA
A14	AVSS45_VPA	GND	VPA ground
B14	VPA_FB	I	BUCK VPA feedback pin
C15	AVDD45_SMPS	PWR	Power supply of buck controller
B16	AVSS45_SMPS	GND	Ground of buck controller
D5,E5,E6,E7,E8,E9,E10,E11,E12,F11,F12,G6,G7,G8,G9,G10,G11,G12,H6,H7,H8,H9,H10,H11,H12,J6,J7,J8,J9,J10,J11,K7,K8,K9,K10,K11,L7,L8,L9,L10,L11,L12	AVSS45_LDO	GND	LDO ground
T13	AVDD45_LDO1	PWR	Power supply input of LDO group1
T8	AVDD45_LDO2	PWR	Power supply input of LDO group2
K1	AVDD45_LDO3	PWR	Power supply input of LDO group3
T11	AVDD45_LDO4	PWR	Power supply input of LDO group4
M2	AVDD45_LDO5	PWR	Power supply input of LDO group5
H3	AVDD22_LDO1	PWR	Power supply input of SYS LDO group1
J2	AVDD22_LDO1	PWR	Power supply input of SYS LDO group1
E1	AVDD22_LDO2	PWR	Power supply input of SYS LDO group2
F1	AVDD22_LDO3	PWR	Power supply input of SYS LDO group3
G1	AVDD22_LDO4	PWR	Power supply input of SYS LDO group4
P9	VTCXO_0	O	VTCXO_0 output voltage
T16	VTCXO_1	O	VTCXO_1 output voltage
F10	VRF18_0	O	VRF18_0 output voltage
F9	VRF18_1	O	VRF18_1 output voltage
J1	VM	O	VDRAM output voltage
E4	VSRAM	O	VSRAM output voltage
H2	VCAMD	O	VCAMD output voltage
T14	VCAMA	O	VCAMA output voltage
E3	VCAMIO	O	VCAMIO output voltage

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Ball	Symbol	I/O	Description
H5	VCAMAF	O	VCAMAF output voltage
F2	VIO18	O	VIO18 output voltage
K2	VIO28	O	VIO28 output voltage
K4	VMC	O	VMC output voltage
R9	VMCH	O	VMCH output voltage
R10	VEMC_3V3	O	VEMC_3V3 output voltage
T15	VEFUSE	O	VEFUSE output voltage
P11	VUSB33	O	VUSB33 output voltage
R11	VSIM1	O	VSIM1 output voltage
N11	VSIM2	O	VSIM2 output voltage
F3	VCN18	O	VCN18 output voltage
R13	VCN28	O	VCN28 output voltage
R12	VCN33	O	VCN33 output voltage
R14	VAUD28	O	VAUD28 output voltage
R15	VAUX18	O	VAUX18 output voltage
H4	VGP1	O	VGP1 output voltage
J4	VIBR	O	VIBR output voltage
E2	PWRKEY	I	PWRKEY button
D2	EXT_PMIC_EN	O	Ext PMIC enable pin
D3	RESETB	O	System reset release signal
M7	WDTRSTB_IN	I	Watchdog reset from AP
D4	PMU_TESTMODE	I	PMU test mode signal (tied to GND in normal operation)
L4	VREF	O	Bandgap reference voltage
L3	AVSS45_VREF	GND	Ground for bandgap
N5	SPI_MISO	IO	SPI control interface
L6	SPI_MOSI	IO	SPI control interface
K6	SPI_CLK	I	SPI control interface
M6	SPI_CSN	IO	SPI control interface
N2	UVLO_VTH	I	UVLO threshold control pin
N6	HOMEKEY	I	HOMEKEY button
P4	FSOURCE	PWR	EFUSE power source
P8	SRCLKEN_IN0	I	Source clock enable pin 0
R5	SRCLKEN_IN1	I	Source clock enable pin 1
M12	AVDD18_AUXADC	PWR	1.8V power supply of AUXADC
M14	ACCDET	I	Accessory detection input
P14	AUXADC_VIN	I	AUXADC input
N13	AVSS18_AUXADC	GND	AUXADC ground
N3	BATSNS	I	Negative terminal for battery's charging current sensing resistor
N4	ISENSE	I	Positive terminal for battery's charging current sensing resistor
M4	VSYSSNS	PWR	VSYS supply input for internal block and UVLO detection
N1	CHG_DP	I	USB D+ for BC1.x standard
M1	CHG_DM	I	USB D- for BC1.x standard
D15	CS_P	I	Fuel gauge ADC input pin

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Ball	Symbol	I/O	Description
E15	CS_N	I	Fuel gauge ADC input pin
J5	FCHR_ENB	I	Force charging disable pin
P13	TREF	O	TREF output voltage
R1	VCDT	I	Fractional charger input voltage for charger detection
R2	VDRV	O	Charger current drive output
P2	BATON	I	Battery NTC pin for battery and its temperature sensing
P3	CHRLDO	O	CHRLDO output voltage
R8	AVDD28_RTC	O	RTC LDO output. Supply of RTC macro where backup battery can be added.
R7	AVSS28_RTC	GND	RTC ground
T6	XIN	IO	32K crystal connection port while using crystal to generate 32kHz clock
R6	XOUT	IO	32K crystal connection port while using crystal to generate 32kHz clock
T1	XOSC_EN	O	XOSC_EN control of RF chip
R3	ENBB	O	ENBB control of RF chip
M9	RTC32K_2V8	O	VRTC domain 32kHz clock output
P5	RTC32K_1V8_0	O	VIO18 domain 32kHz clock output
R4	RTC32K_1V8_1	O	VIO18 domain 32kHz clock output
R16	ISINK0	IO	ISINK channel 0
P15	ISINK1	IO	ISINK channel 1
N14	AVSS45_ISINK	GND	ISINK ground
T2	DVDD18_IO	PWR	Digital IO power
T3	DVDD18_DIG	O	VDIG18 output voltage
T5	DVSS18_IO	GND	Digital IO ground
F15	AU_FLYN	O	Flying capacitor bottom
G15	AU_FLYP	O	Flying capacitor top
H14	AU_REFN	GND	Audio reference ground
F13	AVSS18N_AUD	PWR	Audio -1.8V supply
G13	AVDD18_AUD	PWR	1.8V power supply of Audio
G14	AVSS18_AUD	GND	Audio DL ground
F16	SPK_P	O	Positive output of internal speaker amp
E16	SPK_N	O	Negative output of internal speaker amp
N15	AU_MICBIAS1	O	Microphone Bias 1
N16	AU_MICBIAS0	O	Microphone Bias 0
D14	AVDD45_SPK	PWR	Power supply of SPK
E14	AVSS45_SPK	GND	GND of internal speaker amp
M15	AU_VIN0_N	I	Microphone channel 0 negative input
M16	AU_VIN0_P	I	Microphone channel 0 positive input
L13	AU_VIN1_N	I	Microphone channel 1 negative input
K13	AU_VIN1_P	I	Microphone channel 1 positive input
L14	AU_VIN2_N	I	Microphone channel 2 negative input
K14	AU_VIN2_P	I	Microphone channel 2 positive input
H15	AU_HPL	O	Earphone left channel output
H16	AU_HPR	O	Earphone right channel output

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Ball	Symbol	I/O	Description
J12	CLK26M	I	26MHz clock input
J14	AU_HSN	O	Handset negative output
K15	AU_HSP	O	Handset positive output
M10	AUD_DAT_MISO	IO	Audio control interface
N8	AUD_DAT_MOSI	IO	Audio control interface
K12	AVSS28_AUD	GND	Audio UL ground
K16	AVDD28_AUD	PWR	2.8V supply of Audio UL
M8	AUD_CLK	I	Audio control interface

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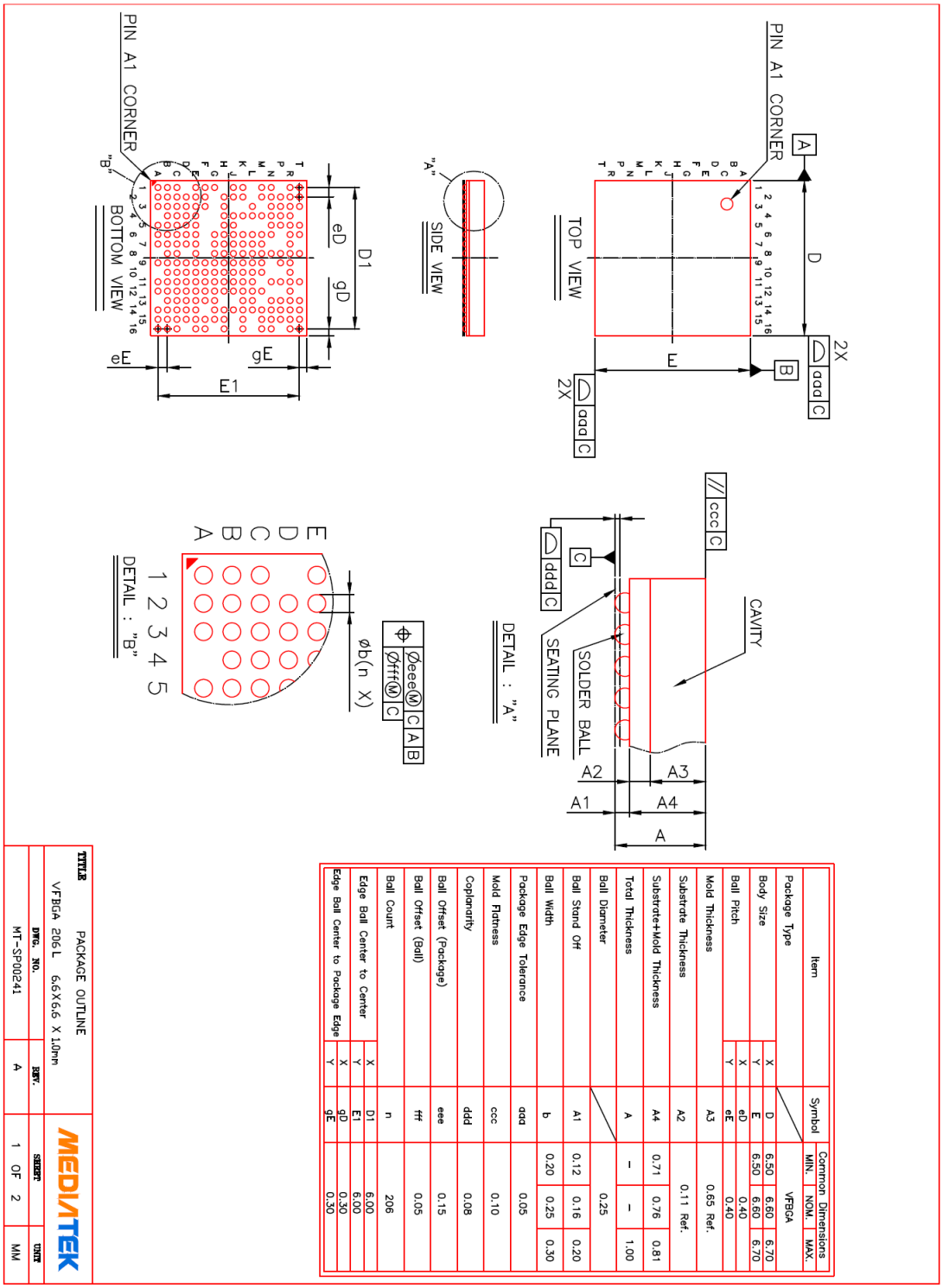
2 MT6328 Packaging

2.1 Package Dimensions



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			VFBGA		
Body Size	X	D	6.50	6.60	6.70
	Y	E	6.50	6.60	6.70
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.65 Ref.	
Substrate Thickness		A2		0.11 Ref.	
Substrate+Mold Thickness		A4	0.71	0.76	0.81
Total Thickness		A	–	–	1.00
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		206	
Edge Ball Center to Center	X	D1		6.00	
	Y	E1		6.00	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

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Appendix

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