

Preliminary

TOSHIBA Photocoupler GaAlAs IRED + Photo IC

TLP350

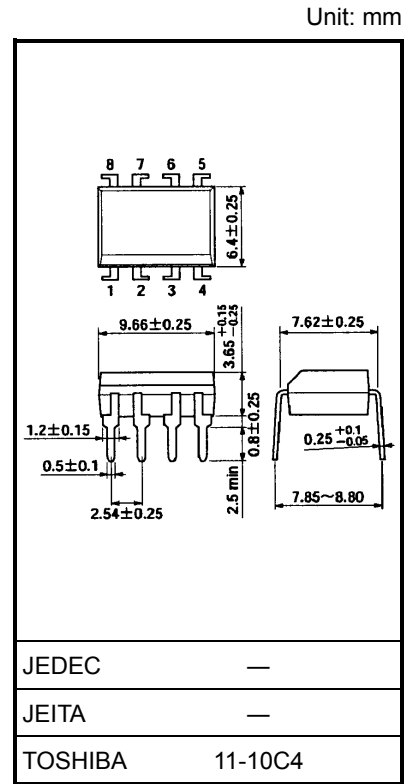
Inverter for Air Conditioner
 IGBT/Power MOS FET Gate Drive
 Industrial Inverter

The TOSHIBA TLP350 consists of a GaAlAs light emitting diode and a integrated photodetector.
 This unit is 8-lead DIP package.
 TLP350 is suitable for gate driving circuit of IGBT or power MOS FET..

- Peak output current: $I_O = \pm 2.0$ A (max)
- Guaranteed performance over temperature: -40 to 100°C
- Supply current: $I_{CC} = 2$ mA (max)
- Power supply voltage: $V_{CC} = 15$ to 30 V
- Threshold input current : $I_{FLH} = 5$ mA (max)
- Switching time (t_{pLH}/t_{pHL}) : 500 ns (max)
- Common mode transient immunity: 15 kV/ μs
- Isolation voltage: 3750 Vrms

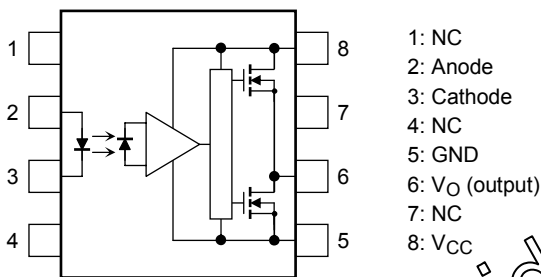
Truth Table

Input	LED	Tr1	Tr2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

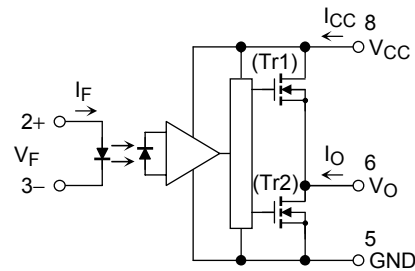


Weight: 0.54 g (typ.)

Pin Configuration (top view)



Schematic



A 0.1 μF bypass capacitor must be connected between pin 8 and 5. (See Note 6)

Development idea
 Not fixed yet

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
LED	Forward current	I_F	20	mA
	Forward current derating (Ta ≥ 85°C)	$\Delta I_F / \Delta T_a$	-0.54	mA/°C
	Peak transient forward current (Note 1)	I_{FP}	1	A
	Reverse voltage	V_R	5	V
	Junction temperature	T_j	125	°C
Detector	"H" peak output current (Note 2)	I_{OPH}	-2.0	A
	"L" peak output current (Note 2)	I_{OPL}	2.0	A
	Output voltage (Note 3)	V_O	35	V
	Supply voltage (Note 3)	V_{CC}	35	V
	Junction temperature	T_j	125	°C
Operating frequency (Note 4)	f			kHz
Storage temperature range	T_{stg}	-55 to 125		°C
Operating temperature range	T_{opr}	-40 to 100		°C
Lead soldering temperature (10 s) (Note 5)	T_{sol}	260		°C
Isolation voltage (AC, 1 minute, R.H. ≤ 60%) (Note 6)	BV_S	3750		Vrms

Note 1: Pulse width $P_W \leq 1 \mu s$, 300 pps

Note 2: Exponential waveform pulse width $P_W \leq \mu s$, $f \leq$ kHz

Note 3: $T_a \leq 100$ °C

Note 4: Exponential waveform $I_{OPH} \leq$ A ($\leq \mu s$), $I_{OPL} \leq +$ A ($\leq \mu s$), $T_a =$ °C

Note 5: It is 2 mm or more from a lead root.

Note 6: Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Note 7: A ceramic capacitor(0.1 μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property.
The total lead length between capacitor and coupler should not exceed 1 cm.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Input current, ON (Note 8)	I_F (ON)	7.5	—	10	mA
Input voltage, OFF	V_F (OFF)	0	—	0.8	V
Supply voltage	V_{CC}	15	—	30	V
Peak output current	I_{OPH}/I_{OPL}	—	—	± 1.0	A
Operating temperature	T_{opr}	-40	—	100	°C

Note 8: Input signal rise time (fall time) < 0.5 μs .

Electrical Characteristics (Ta = -40 to 100°C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit	
Forward voltage		V _F	—	I _F = 5 mA, Ta = 25°C	—	1.55	1.70	V	
Temperature coefficient of forward voltage		ΔV _F /ΔTa	—	I _F = 5 mA	—	-2.0	—	mV/°C	
Input reverse current		I _R	—	V _R = 5 V, Ta = 25°C	—	—	10	μA	
Input capacitance		C _T	—	V = 0, f = 1 MHz, Ta = 25°C	—	45	—	pF	
Output current (Note 9)	"H" Level	I _{OPH1}	1	V _{CC} = 30 V I _F = 5 mA	V ₈₋₆ = 4.0 V	-1.0	-1.5	—	A
		I _{OPH2}			V ₈₋₆ =			—	
	"L" Level	I _{OPL1}	2	V _{CC} = 30 V I _F = 0 mA	V ₆₋₅ = 2.0 V	1.0	2.0	—	
		I _{OPL2}			V ₆₋₅ =			—	
Output voltage	"H" Level	V _{OH}	3	V _{CC} 1= +15 V	I _O = -100 mA, I _F = 5 mA	11	—	V	
	"L" Level	V _{OL}	4	V _{EE} 1= -15 V	I _O = 100 mA, V _F = 0.8 V	—	1.0		
Supply current	"H" Level	I _{CCH}	5	V _{CC} = 30 V V _O open	I _F = 10 mA	—	2.0	mA	
	"L" Level	I _{CCL}	6		I _F = 0 mA	—	2.0		
Threshold input current	L → H	I _{FLH}	—	V _{CC} 1= +15 V V _{EE} 1= -15 V, V _O > 0 V	—	—	5	mA	
Threshold input voltage	H → L	V _{FHL}	—	V _{CC} 1= +15 V V _{EE} 1= -15 V, V _O < 0 V	0.8	—	—	V	
Supply voltage		V _{CC}	—	—	15	—	30	V	
UVLO thresh hold		V _{UVLO+}	—	V _O > 2.5 V, I _F = 5 mA, I _O = 100 mA	11.0	—	13.5	V	
		V _{UVLO-}	—		9.5	—	12.0	V	

*: All typical values are at Ta = 25°C

Note 9: Duration of I_O time ≤ 50 μs

Note 10: This product is more sensitive than the conventional product to static electricity (ESD) because of a lowest power consumption design.

General precaution to static electricity (ESD) is necessary for handling this component.

Isolation Characteristics (Ta = 25°C)

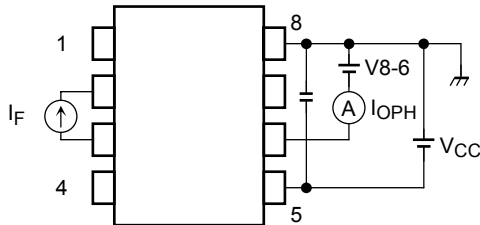
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Capacitance input to output	C _S	V = 0, f = 1MHz (Note6)	—	0.8	—	pF
Isolation resistance	R _S	V _S = 500 V, Ta = 25°C, R.H. ≤ 60% (Note6)	1×10 ¹²	10 ¹⁴	—	Ω
Isolation voltage	BV _S	AC, 1 minute	3750	—	—	V _{rms}
		AC, 1 second, in oil	—	10000	—	
		DC, 1 minute, in oil	—	10000	—	V _{dc}

Switching Characteristics (Ta = -40 to 100°C, unless otherwise specified)

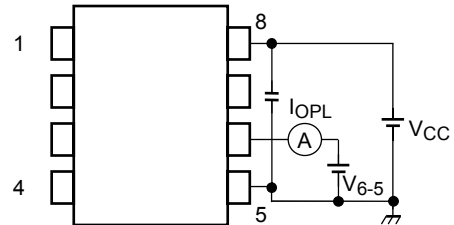
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit	
Propagation delay time	L → H	7	$V_{CC1} = +15\text{ V}$ $V_{EE1} = -15\text{ V}$ $R_g = 20\ \Omega$ $C_g = 10\text{ nF}$	$I_F = 0 \rightarrow 5\text{ mA}$	50	250	500	ns
	H → L			$I_F = 5 \rightarrow 0\text{ mA}$	50	250	500	
Propagation delay difference between any two parts or channels	PDD $ t_{pHL} - t_{pLH} $	8	$V_{CC1} = +15\text{ V}, V_{EE1} = -15\text{ V}$ $R_g = 20\ \Omega$ $C_g = 10\text{ nF}$		—	—	450	ns
Output rise time (10-90%)	t_r				$I_F = 0 \rightarrow 5\text{ mA}$	—	—	—
Output fall time (90-10%)	t_f		$I_F = 5 \rightarrow 0\text{ mA}$	—	—	—		
Common mode transient immunity at high level output	CM_H	8	$V_{CM} = 1000\text{ V}_{p-p}$ $T_a = 25^\circ\text{C}$ $V_{CC} = 30\text{ V}$	$I_F = 5\text{ mA}$ $V_O(\text{min}) = 26\text{ V}$	-15000	—	—	V/ μs
Common mode transient immunity at low level output	CM_L			$I_F = 0\text{ mA}$ $V_O(\text{max}) = 1\text{ V}$	15000	—	—	

*: All typical values are at Ta = 25°C

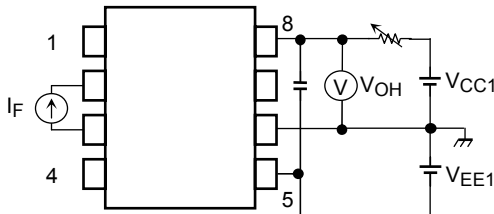
Test Circuit 1: I_{OPH}



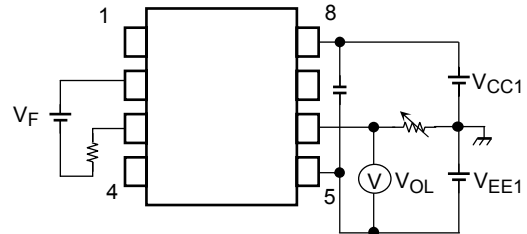
Test Circuit 2: I_{OPL}



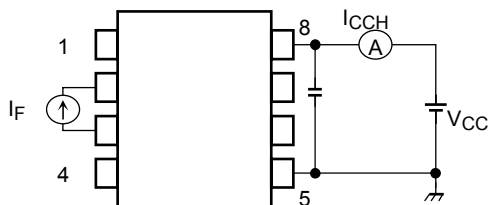
Test Circuit 3: V_{OH}



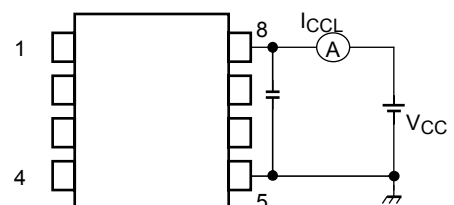
Test Circuit 4: V_{OL}



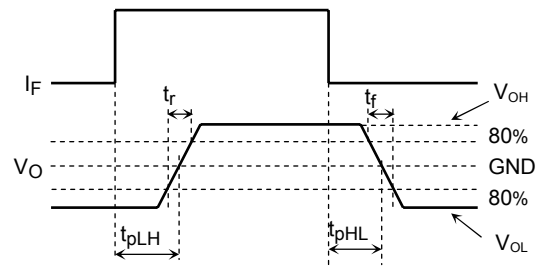
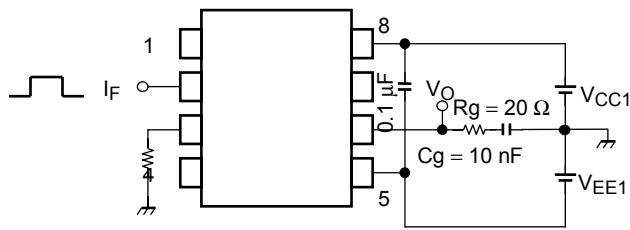
Test Circuit 5: I_{CCH}



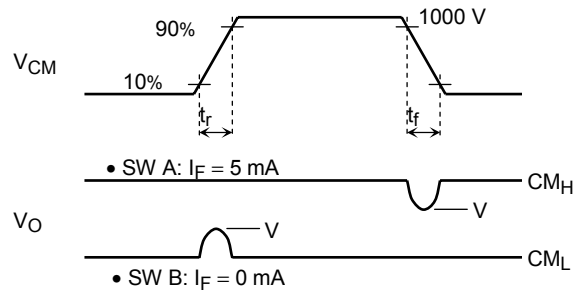
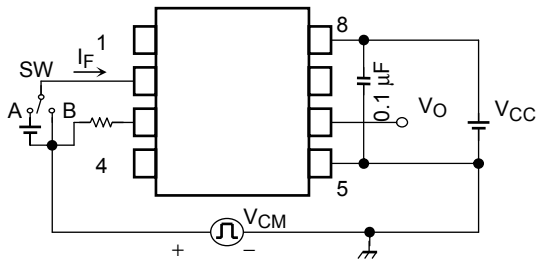
Test Circuit 6: I_{CCL}



Test Circuit 7: t_{pLH} , t_{pHL} , t_r , t_f , PDD



Test Circuit 8: CM_H , CM_L



$$CM_L = \frac{800 \text{ V}}{t_f (\mu\text{s})}$$

$$CM_H = \frac{800 \text{ V}}{t_r (\mu\text{s})}$$

CM_L (CM_H) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

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